An atom chip for the manipulation of ultracold atoms

O. Cherry, J.D. Carter, and J.D.D. Martin

Abstract: We have fabricated an atom chip that magnetically traps laser cooled ^{87}Rb by generating high magnetic-field gradients using micrometre scale current-carrying wires. The wires are fabricated on a Si wafer (with a 40 nm SiO_2 layer) using 1.2 μm thick Au and a 20 nm thick adhesion layer, and are patterned with lift-off photolithography. We characterize the number and temperature of the cold atoms trapped by the chip.

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Résumé : Nous avons fabriqué un micropiège magnétique pour capturer des atomes de ^{87}Rb refroidis par laser, en générant de forts gradients de champ magnétique grâce à des courants circulant dans des fils à l'échelle du micron. Les fils sont fabriqués sur une gaufrette de Si (avec une couche de 40 nm de SiO_2) en utilisant de l'or de 1,2 μm d'épaisseur et une couche épaisse d'adhésif, selon un patron obtenu par photolithographie. Nous déterminons le nombre et la température des atomes froids prisonniers du piège.

[Traduit par la Rédaction]

1. Introduction

A magnetic microtrap, or *atom chip* [1, 2] is an important component for our planned experiments at the University of Waterloo to study the interactions between Rydberg atoms and metal surfaces. These allow a cloud of atoms to be positioned at arbitrary atom–surface distances. There, they can be excited to Rydberg states and interactions between the atoms and the surface of the chip can be measured using shifts and broadenings of the excitation spectra.

Atom chips use miniaturized magnetic potentials to confine samples of cold atoms, exploiting the interaction between paramagnetic atoms and inhomogeneous magnetic fields. They are are extremely versatile tools for the study of quantum gases, matter-wave interferometry, and atom–surface interactions. See refs. 3–6 for a comprehensive review of atom chip design, fabrication, and experiments.

The interaction, between an atom with a magnetic moment, $\bar{\mu}$, and a magnetic field, $\bar{B}$, leads to the potential.

$$V_B = -\bar{\mu} \cdot \bar{B} \tag{1}$$

For adiabatically (slowly) varying fields, the potential is

$$V_B = \mu_B g_F m_F B \tag{2}$$

where μ_B is the Bohr magneton (>0), g_F is the Landé factor, and m_F is the magnetic quantum number. A magnetic field minimum can form a trap for neutral atoms in a *weak field-seeking* state ($g_F \cdot m_F > 0$). A simple two-dimensional trap can be created by combining the field from a straight current-carrying wire with a homogeneous perpendicular bias field [7]. At a certain distance from the wire the two fields cancel, resulting in a line of zero field parallel to the wire at

$$r_0 = \frac{\mu_0 I}{2\pi B_b} \tag{3}$$

where I is the wire current and B_b is the magnitude of the bias field (see Fig. 1). The position of r_0 can be controlled by varying I and B_b, allowing for precise positioning of the trap centre. A three-dimensional trap can be formed by kinking the ends of the wire into a U or S shape [1].

An atom chip uses micrometre-scale wires, fabricated on a substrate, to generate trapping potentials using these principles [1, 8]. The small wire cross sections allow for higher potential gradients to form tighter traps and the thermal contact between the wires and the substrate increases the sustainable current densities. The substrate also provides structural rigidity for the wires. Many of the processes used in atom-chip fabrication are common to the manufacturing of semiconductor devices, making complex wire patterns and thus complex trapping potentials possible.

In this article, we present the design, fabrication, and performance of an atom chip fabricated entirely at the University of Waterloo. A requirement of our project is the ability to fabricate atom chips *in house* to reduce wait times and costs involved with design updates or the replacement of a damaged chip. For this reason, we have developed our own fabrication processes using the Centre for Integrated RF Engineering (CIRFE) facility at the University of Waterloo. The primary purpose of this chip is to gain experience with magnetic trapping of ^{87}Rb.

With this first generation atom chip we have developed a procedure for loading the atoms from a background vapour into the magnetic microtrap through a series of intermediate

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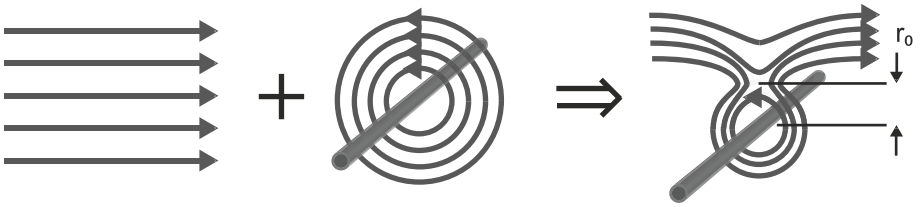
Fig. 1. Magnetic field formed by a straight current-carying wire and a perpendicular bias field. At a position, r_0, from the wire centre, the two fields cancel, resulting in a field minimum.



trapping steps. Using RF (radio frequency) evaporation, we have cooled the atoms to create well-localized dense clouds of atoms suitable for Rydberg atom–surface interaction studies.

2. Design

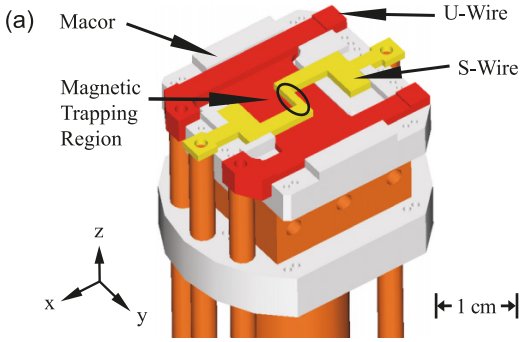
Our system uses a magneto-optical trap (MOT) [9] for cooling and collecting the ^{87}Rb from a background vapour. A conventional MOT requires six beams in three orthogonal counterpropagating pairs. Trapping atoms close to the surface of the chip using six beams is difficult due to limited optical access. Instead, we use the surface of the chip as a reflector for two of the beams requiring just four incoming beams. This setup is known as a *mirror* MOT [1].

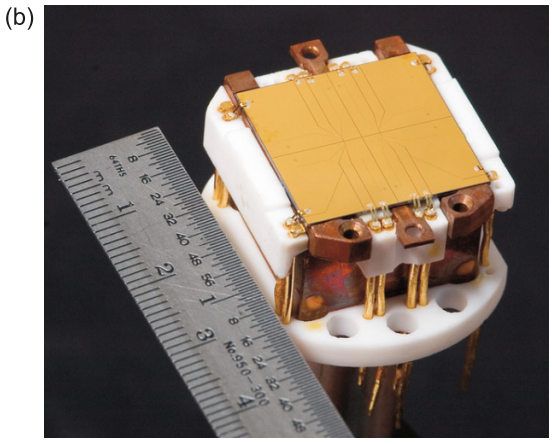
To generate the quadrupole field we use a copper U-shaped conductor, set beneath the chip, and external Helmholtz coils as described in ref. 10 (see Fig. 2*a*). The centre section of the U-wire is 14 mm long with a 1 × 9 mm cross section. The flat wire spreads out the current flow and, when combined with an inclined bias field, forms a field that more closely resembles an ideal quadrupole than is possible with a simple U-wire. A 1 × 1 mm copper S-shaped wire, 2.8 mm long, is positioned between the U-wire and the chip (the S-shaped wire is often referred to as a Z-wire [1]). The S-wire is used to form a purely magnetic, intermediate trap for loading the chip from the mirror MOT. The U- and S-wires are embedded in a piece of machined Macor®, that also holds banks of Au pins for electrical connections to the chip.

The atom chip has dimensions of 2.02 × 2.02 cm, as it is required to pass through a 2.75 in (1 in = 2.54 cm) Conflat port on the vacuum chamber. Since the chip surface must be reflective it is coated uniformly with Au, with thin gaps to define the wires. The fields for the magnetic trap are formed by five parallel wires at the centre of the atom chip (see Fig. 3). The centre wire is H-shaped, allowing it to function as either an S- or a U-wire ($C_{1–4}$). A U-shaped wire lies on each side of the centre wire ($UI_{1–2}$, $UI_{3–4}$). This pair of wires forms the bias field when trapping with the centre wire. They also act in conjunction with the centre wire to load the chip from the macroscopic S-wire trap, with the three carrying copropagating currents. The outermost wires ($UO_{1–2}$, $UO_{3–4}$) are U-shaped and generate the bias field when loading atoms from the S-wire trap. Each of the wires ends in a bond pad at the edge of the chip.

With the centre wire used in the S- configuration, the chip may be used to produce a Ioffe–Pritchard microtrap. The ends of the wire contribute to the Ioffe–Pritchard field (the field along the long axis of the trap — the longitudinal direction), but an additional homogeneous magnetic field is added with macroscopic external coils outside of the vacuum chamber. This field helps prevent loss from the trap due to nonadiabatic spin flips. The resulting trap is harmonic in all three dimensions for small displacements from its center.

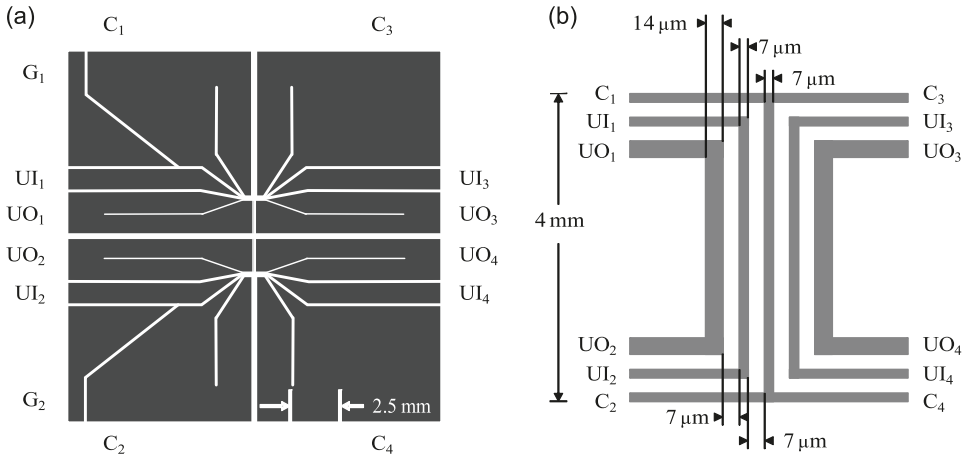
Fig. 2. (*a*) The submount below the chip showing the macroscopic U- and S-wires embedded in a Macor® block. The atom chip rests on this structure, making contact with the top surfaces of both wires. The area of the S-wire above which atoms are magnetically trapped is marked with an oval. (*b*) Image of the atom chip mounted on the substructure. The ribbon bonds can be seen around the perimeter of the chip. In this image, electrical connections to the U- and S-wires have yet to be made.





Compared to other microtraps, the chip presented here has much less confinement in the longtitudinal direction. This is because the chip is intended for the study of Rydberg-atom–surface interactions. We wish to obtain relatively large signal levels, but must minimize Rydberg atom – Rydberg atom interactions. However, the disadvantage of such weak confinement is that evaporative cooling is less efficent. This chip is not suitable for the production of quantum degenerate gases.

Fig. 3. Schematic of the atom chip. (*a*) Trapping wires, with bond pads labelled around the perimeter. (*b*) Magnified view of the centre section of the chip (note that the horizontal and vertical scales differ).



3. Fabrication

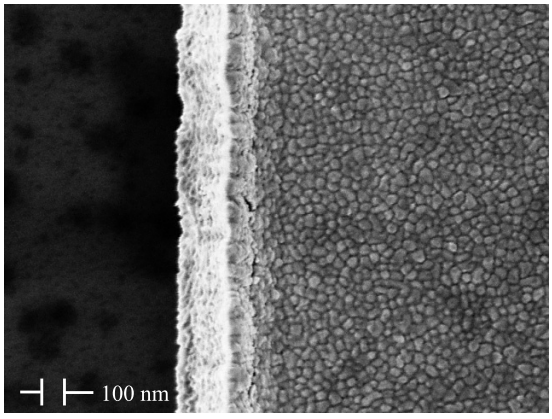
Our atom chip is fabricated using lift-off photolithography [11] on a 0.5 mm thick Si substrate. The wafer is commercially coated with a 40 nm thermally-grown SiO_2 which insulates electrically, but has been shown to be thin enough to provide sufficient thermal contact to the substrate [12]. The wires are Au, 1.2 μm thick, with a thin (10–20 nm) underlying layer of Cr for adhesion between the Au and SiO_2. Lift-off photolithograpy, as opposed to electroplating and wet chemical etching, produces wires with smooth sidewalls [12]. Minimal sidewall roughness is important to generating smooth trapping potentials, as described later in this section.

Before patterning, the wafer is first cleaned using the RCA 1 process (5:1:1 H_2O:NH_4OH:H_2O_2, see ref. 13) to remove unwanted organic contamination that may have occurred during storage. The wires are patterned using AZ 2035 *n*LOF negative photoresist (AZ Electronic Materials, Branchburg, NJ). The photoresist is spun at 2000 RPM for 30 s to give a thickness of about 4 μm and baked at 110 °C for 60 s. The resist is exposed for 12 s using an Oriel mask aligner and a custom-made Cr mask. After exposure, the photoresist is again baked at 110 °C for 60 s and developed in AZ 300 MIF for 120 s.

The metal films are deposited by electron beam evaporation (Nanochrome PVD system, Intlvac, Toronto, ON). The deposition rate for Au is 10 Å/s and for Cr is 3 Å/s. After metallization, the chip is soaked in warm acetone for 30 min to dissolve the photoresist and remove the unwanted metal. A 30 min soak in AZ Kwik Strip photoresist remover strips any remaining hardened resist. If necessary, a low-power ultrasonic clean in isopropanol can remove metal flakes that may have clung to the surface.

Once complete, the wafer is diced to size. The atom chip is then glued to the top surfaces of the U- and S-wires (embedded in the Macor® block) using vacuum-compatible epoxy (Epo-tek 353ND, Epoxy Technology, Billerica, MA). The chip is connected to the pins in the Macor® with Au ribbon (25 × 250 μm) using an ultrasonic wedge bonder (Model 4523, K&S, Fort Washington, PA). A small bead of Epo-tek H21D silver-filled epoxy is applied to strengthen each bond. An image of a completed and mounted chip can be seen in Fig. 2*b*).

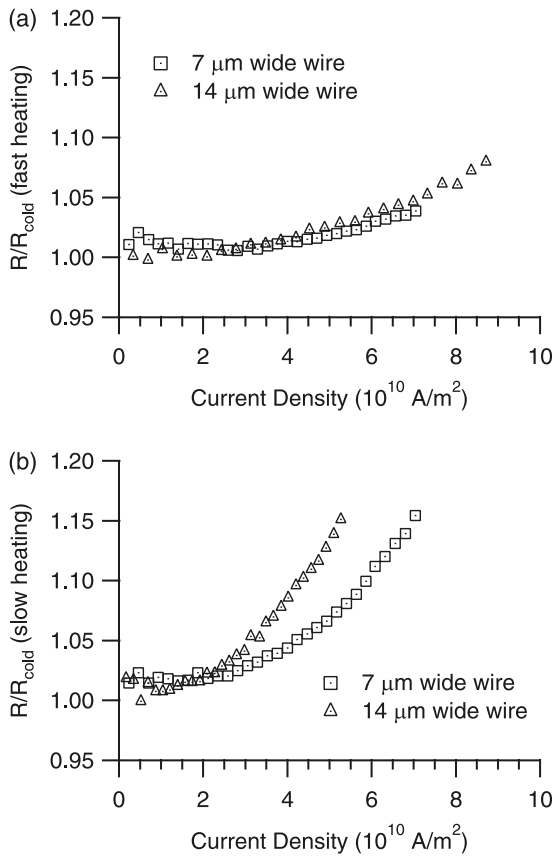
Fig. 4. SEM image of the edge of a wire, showing a grain diameter of approximately 50 nm. The lateral deviations in the wire edge are less than 100 nm.



Trapping wire edge roughness causes the current to stray from a straight path, generating a corrugated axial component to the magnetic field and fragmentation of the trapped atom cloud [14, 15]. Figure 4 shows a scanning electron microscope (SEM) image of a wire edge. The edge deviations are less than 100 nm, and are close to the 50 nm average grain diameter of the gold film. Kruger et al. [16] did a comprehensive study of the potential roughness due to wire imperfections for wires similar to ours (fabricated using lift-off photolithography and gold evaporation). They found a similar edge roughness. With thermal clouds of atoms at temperatures above 1 mK they observed smooth longitudinal density profiles for the trapped atoms down to distances 2 mm away from the wire. As our Rydberg atom studies are planned for greater distances (>10 μm) and temperatures, we do not expect significant density inhomogeneities in the trapped atom cloud due to wire roughness.

High current densities are required when loading from the S-wire trap and when trapping atoms close to the surface of the chip. We have measured heating in the wires of a chip under vacuum at current densities up to 9×10^{10} A/m^2. Heating may be understood as occurring on two qualitatively different time scales: one in which the contact resistance between the wires and substrate is important, and a

Fig. 5. Resistance increase due to wire heating for 7 and 14 μm wires under vacuum. (*a*) Fast timescale, measured at 0.5 ms after the start of the current pulse. (*b*) Slow timescale, measured at 500 ms after the start of the current pulse.



longer timescale where the thermal conductivity of the substrate is significant. The fast timescale corresponds to several hundred microseconds, whereas the slow timescale is hundreds of milliseconds and longer. Wire heating (measured using the wire resistance) on the two time-scales is shown in Fig. 5. The slow heating behaviour is similar to the chips fabricated by Groth et al. [12]. Under vacuum, the 7 and 14 μm wires can withstand 500 ms pulses with current densities of 7×10^{10} A/m^2 and 5×10^{10} A/m^2, respectively. Slow heating under vacuum up to these currents matches measurements made in air, suggesting that higher currents are achievable without damaging the wires.

4. Performance

Our approach to the mirror MOT and magnetic trapping is adapted from well-established designs [10, 17]. The mirror MOT uses the ^{87}Rb D_2 line for cooling and trapping. For a frequency reference, a home-built diode laser is locked to the $F = 2 \rightarrow F' = 3$ transition using polarization spectroscopy [18]. The cooling and trapping (CT) laser (Toptica DLX 110) and repump laser (Toptica DL 100) are locked to the reference laser using beatnote locking [19]. The CT beam is split into two additional beams to be used for optical pumping and absorption imaging. Acousto-optic modulators (AOMs) are used for frequency shifting and switching.

We typically trap 1.5–2.0 $\times$ 10^7 atoms in the mirror MOT. Once the MOT is loaded, the trap is compressed and moved towards the chip. The cloud is cooled to 40 μK by ramping the magnetic fields to near zero, decreasing the laser power and detuning the CT frequency to form an optical molasses [20]. Temperature is measured using the ballistic expansion method (see, for example, ref. 21). The atoms are optically-pumped into the $|F = 2,\ m_F = 2>$ weak-field-seeking state using a branch of the CT beam. The quantization axis is defined by an applied magnetic field from external coils.

The currents in the S-wire and the bias field coils are ramped up to form the macroscopic magnetic trap, which is then compressed and moved towards the chip (1.0×10^7 to 1.5×10^7 atoms).

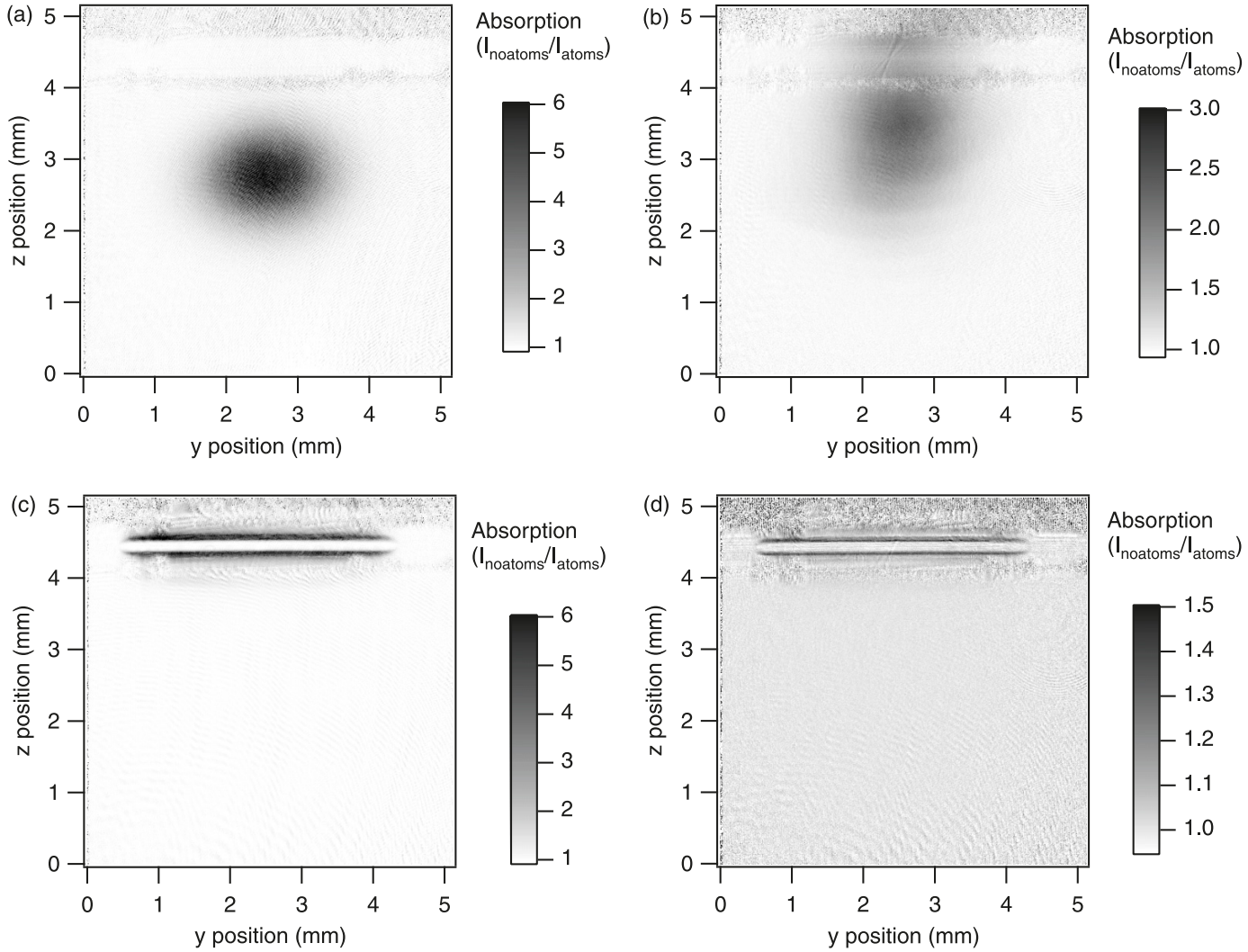
The chip trap is loaded by ramping up the currents in the chip wires (all wires carrying current in the same direction) and then ramping down the current in the S-wire. In this configuration, the trap minimum is approximately 60 μm from the surface and the trap has a radial oscillation frequency of approximately 4 kHz. The potential in the longitudinal direction is more box-like than harmonic at our temperatures. The calculated curvature at the centre of the trap gives a longitudinal frequency of 7 Hz. At the lowest temperatures in this work (150 μK) a harmonic trap of 7 Hz would produce a Gaussian density distribution with a FWHM of 5.2 mm in this dimension. Instead the density is observed to be relatively uniform in this dimension over a length of 3.7 mm (see Fig. 6). The confinement is due to the rapid increase in the Ioffe–Pritchard field at the ends of the central wires.

Approximately 3.5×10^6 to 4.0×10^6 atoms can be loaded into the chip trap. Due to the strong confinement, the temperature of the cloud after transfer to the chip trap is on the order of 1 mK, close to the trap depth of 3.6 mK. In the chip the 1/*e* lifetime is observed to be 0.7 s. The lifetime in the macroscopic S-trap is about 4 s, limited by background-gas collisions. Proximity to a metal surface can lead to thermal magnetic-field noise induced spin-flips. Based on the theory in ref. 22, we estimate the rate to correspond to a lifetime greater than 10 s. The relatively short lifetime observed for the chip trap is possibly due to technical noise in the current supplies.

After transfer to the chip trap, the cloud is cooled by RF evaporation [23]. An RF sweep (near 6.8 GHz) is applied to drive atoms from the trapped $|F = 2,\ m_F = 2>$ state to the untrapped $|F = 1,\ m_F = 1>$ state. The RF is detuned from the zero-field resonance frequency of the transition, so that atoms in the proper local magnetic field (located in a shell surrounding the trap minimum) are Zeeman-shifted into resonance and ejected from the trap. The sweep starts at a high frequency to eject the most energetic atoms so that the cloud is cooled. The sweep has four linear ramps and covers a total frequency range of 70 MHz in 650 ms. At the end of the RF sweep, the effective trap depth is approximately 500 μK. At this point, about 2.0×10^5 atoms remain in the chip trap.

The trapped atoms are counted by an absorption-imaging method similar to that described in ref. 24. The imaging beam, resonant with the $F = 2 \rightarrow F' = 3$ transition, passes through the cloud and is absorbed. The cloud is imaged with an Apogee Alta U260 CCD still camera and a two lens telescope. Figure 6 shows absorption images of trapped atoms at various stages in the chip-loading process.

Fig. 6. Absorption images of the cloud of cold atoms at various points in the experimental sequence: (*a*) After loading the MOT and cooling with optical molasses (1.6×10^7 atoms, 40 μK). (*b*) After transfer to the macroscopic Ioffe–Pritchard trap formed with the S-wire and external coils (1.0×10^7 atoms, 150 μK). The surface of the chip is visible (the region of higher noise, due to the blocked probe) in the top portion of this image. (*c*) After transfer to the microtrap formed with the chip wires and external coils (3.5×10^6 atoms, 1 mK). Two images of the cloud are visible due to reflection from the surface of the chip. (*d*) After 650 ms of RF evaporative cooling in the microtrap (2.0×10^5 atoms, 150 μK).



After RF evaporation, the cloud temperature is 150 ± 10 μK, as measured by ballistic expansion. The cloud is released by ramping down the wire currents and leaving the homogeneous bias field (parallel to the imaging axis) unchanged. The wire currents were ramped down in 10 μs. This is much faster than the mechanical oscillation of the trap (to avoid accelerating the atoms during the shutdown), but slow enough to prevent nonadiabatic transitions to states that cannot scatter light from the imaging beam. Images are taken between 1 and 6 ms after release, a range limited by the imaging resolution for short delay times and the signal and (or) noise of the imaging system for long delays.

We can estimate the peak number density and phase space density from the total number of atoms in the trap and their temperature. The trap is assumed to be to be box-like in the longtitudinal direction (with a length of 3.7 mm) and harmonic in the transverse dimension (with an oscillation frequency of $\omega/(2\pi) = 4$ kHz). Boltzmann statistics for noninteracting particles gives the peak density as $n = 3.8 \times 10^{11}$ cm^{-3} (for 2×10^5 atoms at 150 μK). The phase space density may be computed as $D = n\lambda_{dB}^3$, where $\lambda_{dB} = \sqrt{2\pi^2/(mkT)}$. In our case, $D = 1.3 \times 10^{-6}$. As discussed in Sect. 2, Design, a higher phase space density could be obtained with more confinement in the longtitudinal direction.

5. Discussion

We have fabricated an atom chip at the University of Waterloo and incorporated it into an experimental setup. We have used RF evaporation to produce samples of 2.0×10^5 atoms at temperatures of approximately 150 mK. These samples are sufficiently well-localized and dense to be useful for studies of Rydberg atom–surface interactions.

This is a first generation chip, intended to gain experience with magnetic trapping and perform preliminary spectro-

scopic measurements of Rydberg atoms near a surface. However, Rydberg atoms are strongly perturbed by weak electric fields [25]. We expect that the electric fields created by voltage drops along the wires and the voltage differences between them will make this chip less than ideal for most of our intended experiments. A second generation chip has been fabricated with an evaporated Au *shield layer*, isolated from the wires by a planarizing polyimide film. This chip will be described in a future publication.

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